What is claimed is:

1. An apparatus comprising:

a substrate;

a target timing circuit formed on the substrate, the target timing circuit having a frequency related to a target frequency;

a leakage timing circuit formed on the substrate, the leakage timing circuit having a frequency related to a leakage current; and

a control unit to maintain a substantially constant ratio between the frequency related to the target frequency and the frequency related to the leakage current.

2. The apparatus of claim 1, wherein the substrate comprises a semiconductor.

3. The apparatus of claim 2, wherein the target timing circuit comprises a ring oscillator coupled to a counter.

4. The apparatus of claim 3, wherein the leakage timing circuit comprises a ring oscillator.

5. The apparatus of claim 4, wherein the frequency related to the leakage current is substantially proportional to the leakage current.

6. The apparatus of claim 1, further comprising a self-timed circuit formed on the substrate, the self-timed circuit to operate at a frequency proportional to the target frequency.

7. The apparatus of claim 6, the control unit to provide a control signal to the substrate.

8. The apparatus of claim 6, wherein the substrate includes a plurality of coupled wells containing transistors of a matching type from the self-timed circuit, the target timing circuit, and the leakage timing circuit.

9. The apparatus of claim 8, wherein the transistors are all of the matching type.

10. The apparatus of claim 9, further comprising a well control unit to provide a bias to the plurality of coupled wells.

11. The apparatus of claim 10, wherein the well comprises a *p*-type well.

12. A system comprising:

a substrate;

a target timing circuit formed on the substrate, the target timing circuit having a frequency related to a target frequency;

a leakage timing circuit formed on the substrate, the leakage timing circuit having a frequency related to a leakage current;

a control unit coupled to a flash memory and to maintain a substantially constant ratio between the frequency related to the target frequency and the frequency related to the leakage current; and

a self-timed circuit formed on the substrate, and the self-timed circuit to operate at a frequency proportional to the target frequency.

13. The system of claim 12, wherein the self-timed circuit comprises a memory device communication interface.

14. The system of claim 12, wherein the self-timed circuit comprises a peripheral device communication interface.

15. The system of claim 12, wherein the self-timed circuit comprises a network communication interface.

16. An apparatus comprising:

a substrate;

a self-timed circuit formed on the substrate, the self-timed circuit to operate at a target circuit frequency;

a target timing circuit formed on the substrate, the target timing circuit to generate a signal having a frequency related to the target circuit frequency;

a leakage timing circuit formed on the substrate, the leakage timing circuit having a leakage current and the leakage timing circuit to generate a signal having a frequency related to the leakage current; and

a control unit to receive the signal having the frequency related to the target circuit frequency and the signal having the frequency related to the leakage current and to generate a control signal for application to the substrate, the control signal to maintain a substantially constant ratio between the frequency related to the target circuit frequency and the frequency related to the leakage current.

17. The apparatus of claim 16, wherein the substrate comprises silicon.

18. The apparatus of claim 17, wherein the target circuit comprises an interface circuit.

19. The apparatus of claim 18, wherein the target ring oscillator comprises a ring oscillator coupled to a counter.

20. The apparatus of claim 19, wherein the leakage ring oscillator comprises a delay line.

21. An apparatus comprising:

a substrate;

a synchronous circuit formed on the substrate, the synchronous circuit to operate at a target circuit frequency;

a target timing circuit formed on the substrate, the target timing circuit including voltage control, the target timing circuit to generate a signal having a frequency related to the target circuit frequency;

a leakage timing circuit formed on the substrate, the leakage timing circuit including voltage control, the leakage timing circuit having a leakage current and the leakage timing circuit to generate a signal having a frequency related to the leakage current;

a control unit to receive the signal having a frequency related to the target circuit frequency, the signal having a frequency related to the leakage current, and to generate a control signal for application to the substrate, the control signal to maintain a substantially constant ratio between the frequency related to the target circuit frequency and the frequency related to the leakage current;

a power source to provide a potential to the synchronous, the target timing circuit, and the leakage timing circuit; and

a potential control unit to receive the signal having the frequency related to the target circuit frequency and the signal having the frequency related to the leakage current and to generate a potential control signal to provide to the power source to adjust the potential.

22. The apparatus of claim 21, wherein the substrate comprises silicon.

23. The apparatus of claim 22, wherein the synchronous circuit comprises a processor.

24. The system of claim 23, wherein the processor comprises a very long instruction word processor.

25. The apparatus of claim 21, wherein the control unit includes a low-leakage control signal to set the target circuit to a low leakage state.

26. A method comprising:

generating a first signal related to a target circuit frequency;

generating a second signal related to a leakage current; and

adjusting a control signal applied to a substrate to maintain a substantially constant frequency ratio between the first signal and the second signal.

27. The method of claim 26, further comprising for a processor formed on the substrate and having an operating frequency and a supply voltage, changing the supply voltage to maintain a relationship between the target circuit frequency and the operating frequency.

28. The method of claim 26, further comprising for a communications circuit formed on the substrate, activating a transceiver in the communications circuit.

29. The method of claim 26, further comprising processing the target circuit frequency and a target ring oscillator frequency to generate a potential control signal to adjust a potential applied to a target ring oscillator, a leakage ring oscillator, and a target circuit that operates at the target circuit frequency.

30. The method of claim 29, further comprising for a communications circuit formed on the substrate, activating a transceiver in the communications circuit.